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Establishing a New Benchmark in Quantum Computational Advantage with 105-qubit Zuchongzhi 3.0 Processor

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In the relentless pursuit of quantum computational advantage, we present a significant advancement with the development of Zuchongzhi 3.0. This superconducting quantum computer prototype, comprising 105 qubits, achieves high operational fidelities, with single-qubit gates, two-qubit gates, and readout fidelity at 99.90%, 99.62%, and 99.13%, respectively. Our experiments with an 83-qubit, 32-cycle random circuit sampling on the Zuchongzhi 3.0 highlight its superior performance, achieving 1×10^6 samples in just a few hundred seconds. This task is estimated to be infeasible on the most powerful classical supercomputers, Frontier, which would require approximately 5.9×10^9 yr to replicate the task. This leap in processing power places the classical simulation cost 6 orders of magnitude beyond Google's SYC-67 and SYC-70 experiments [Morvan *et al.*, Nature **634**, 328 (2024)], firmly establishing a new benchmark in quantum

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computational advantage. Our work not only advances the frontiers of quantum computing but also lays the groundwork for a new era where quantum processors play an essential role in tackling sophisticated real-world challenges.

Introduction—The quest for quantum computational advantage has been a central driving force in the field of quantum computing. This term captures the pivotal moment when a quantum computer is capable of executing calculations that are beyond the reach of even the most advanced classical computers [1–9]. In 2019, the Google team developed a 53-qubit superconducting quantum processor named Sycamore [2] to implement random circuit sampling (RCS) [10–12] that they claimed would take the best classical supercomputer 10 000 years. Using a different approach known as Gaussian boson sampling [13,14], in 2020, photons were used to demonstrate quantum computational advantage with 76 photons [6], which was later increased up to 255 photons [7–9].

However, due to rapid advancements in classical algorithms [15–17], the RCS task in Ref. [2] has now been efficiently carried out on GPUs at 2.9% of the initial time cost and with 6.7% of the power consumption required by Sycamore [16,17]. This fact indicates that the quantum computational advantage is not established in a single-shot experiment, but is gradually built upon continuous competition between faster classical simulation and improved quantum devices. Continuous efforts [3–5] have been devoted into developing larger-size and higher-fidelity superconducting quantum processors (see Table I), pushing the boundaries of what is achievable with quantum technologies. To date, the largest scale of RCS reported in literature has been with 67 qubits at 32 cycles (SYC-67) and 70 qubits at 24 cycles (SYC-70) [5].

In this Letter, we aim to challenge this record and establish a new benchmark in quantum computational advantage. We have developed Zuchongzhi 3.0, a more powerful superconducting quantum computer prototype, equipped with 105 qubits and exceptionally high-fidelity manipulation capabilities. The single-qubit gate, two-qubit gate, and readout fidelities are 99.90%, 99.62%, and 99.13%, respectively. Leveraging this prototype, our experiments utilize a significantly larger quantum circuit of 83 qubits at 32 cycles, thereby pushing the limits of current quantum hardware capabilities. On our Zuchongzhi 3.0, the task of obtaining 1×10^6 samples is accomplished in just a few hundred seconds. It is a stark contrast to the estimated 5.9×10^9 years required by the most formidable supercomputers of today, Frontier, to replicate this sampling endeavor. Compared to Google's latest experiment, SYC-67 and SYC-70 [5], the classical simulation cost of our 83-qubit, 32-cycle experiment is 6 orders of magnitude higher. Through this achievement, we establish a new benchmark in quantum computational advantage, which is essential for harnessing the full potential of quantum computing. Beyond this, our work opens avenues for investigating how increases in qubit count and circuit complexity can enhance the efficiency in solving real-world problems.

Zuchongzhi 3.0 quantum processor—The Zuchongzhi 3.0 quantum processor marks a significant upgrade from its predecessor, Zuchongzhi 2.0, with a notable increase in both the quantity and quality of qubits. It now houses 105 transmon qubits, arrayed in 15 rows and 7 columns, forming a two-dimensional rectangular lattice as depicted in Fig. 1. We conducted experiments with a maximum of 83 qubits selected from the processor.

TABLE I. Estimated classical computational cost for different experiments. The Frontier supercomputer boasts a theoretical peak performance of 1.685×10^{18} FLOPS. In our estimations, we presume a 20% FLOP efficiency and convert the machine FLOPS to single-precision complex FLOPS. We provide two scenarios: one with 9.2 PB of memory (the actual memory of Frontier) and another with 762.2 PB (combining Frontier's actual memory with all storage, which is an impractical situation).

| Experiment | Fidelity | Memory constraint: 9.2 PB | | | Memory constraint: 762.2 PB | | |
		1 amplitude (FLOP)	1×10^6 noisy samples (FLOP)	Run-time on Frontier	1 amplitude (FLOP)	1×10^6 noisy samples (FLOP)	Run-time on Frontier
Sycamore-53-20	2.2×10^{-3}	7.2×10^{18}	6.5×10^{16}	1.6 s	5.9×10^{18}	6.1×10^{16}	1.5 s
Zuchongzhi-56-20	6.6×10^{-4}	9.3×10^{19}	2.2×10^{17}	5.3 s	1.0×10^{20}	1.5×10^{17}	3.6 s
Zuchongzhi-60-24	3.7×10^{-4}	3.2×10^{21}	1.6×10^{19}	384.0 s	3.0×10^{21}	2.3×10^{18}	55.2 s
Sycamore-70-24	1.7×10^{-3}	1.7×10^{25}	8.2×10^{25}	62.1 yr	3.2×10^{24}	1.4×10^{24}	1.1 yr
Sycamore-67-32	1.5×10^{-3}	8.2×10^{28}	4.7×10^{27}	3.6×10^3 yr	1.3×10^{26}	9.6×10^{24}	7.2 yr
Zuchongzhi-83-32	2.3×10^{-4}	5.1×10^{31}	7.7×10^{33}	5.9×10^9 yr	1.3×10^{29}	6.9×10^{31}	5.2×10^7 yr

(a)

(b)

(c)
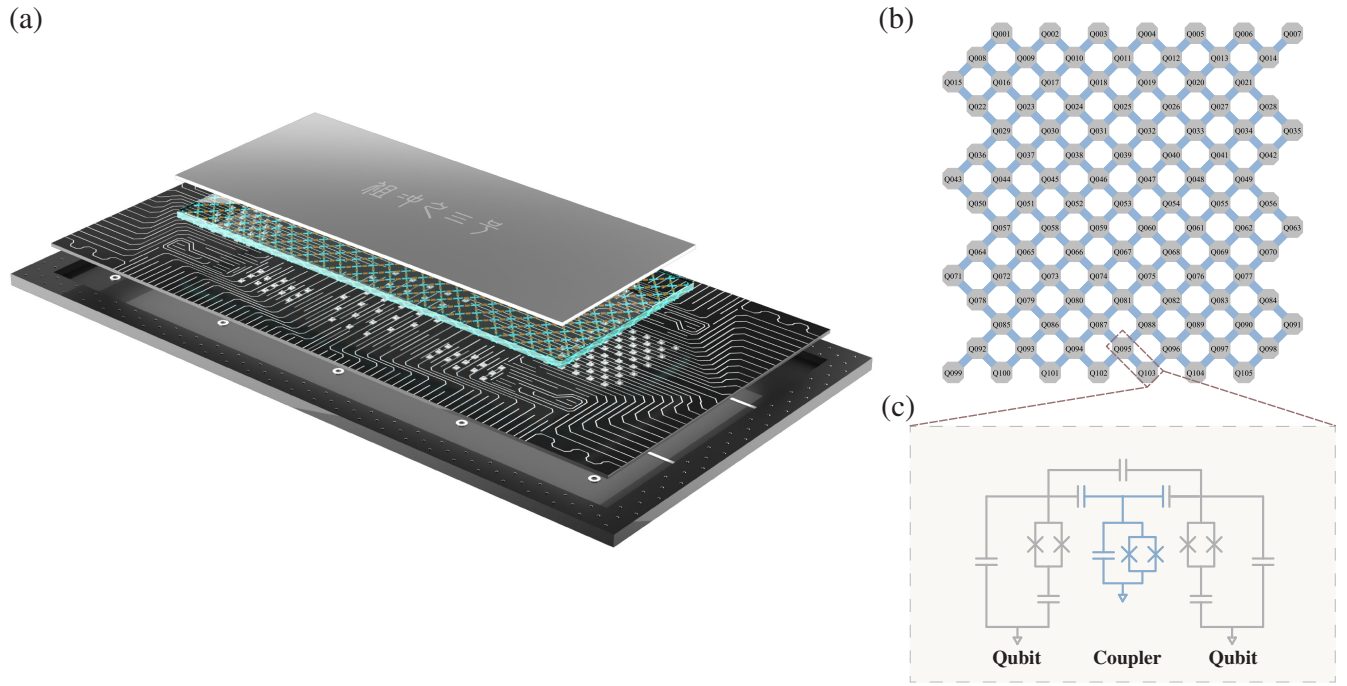
FIG. 1. Zuchongzhi 3.0 quantum processor. (a) The illustration of the Zuchongzhi 3.0 quantum processor. The device consists of two sapphire chips integrated using a flip-chip technique. One chip integrates 105 qubits and 182 couplers, while the other is integrated with all the control lines and readout resonators. (b) The topological diagram of qubits and couplers. Dark gray denotes qubits, light blue denotes couplers. (c) Simplified circuit schematic of two qubits coupled via a coupler.

One of the most significant advancements in the Zuchongzhi 3.0 quantum processor is the enhancement of coherence time. This improvement is achieved through several key strategies. First, we optimize the circuit parameters of the qubits, including the capacitance and the Josephson inductance, to reduce sensitivities to charge and flux noise. Second, we optimize the electric field distribution by modifying the shape of the qubit capacitor pads, which minimizes surface dielectric loss. Third, the attenuator configuration in the wiring is upgraded to mitigate noise from room-temperature electronics, significantly improving the dephasing time. Finally, we update the chip fabrication procedure by lithographically defining base components made of tantalum on the top sapphire substrate and aluminium on the bottom sapphire substrate, which are then bonded together using an indium bump flip-chip technique. This approach reduces the contamination at the interface and enhances the relaxation time of qubits. As a result, we improve the relaxation time (T_1) to 72 µs and the dephasing time ($T_{2,\text{CPMG}}$) to 58 µs, where CPMG represents the Carr-Purcell-Meiboom-Gill sequence.

The calibration processes for single-qubit gates and ISwap-like gates are similar to those employed in Zuchongzhi 2.0. Because of advancements in coherence time, the average Pauli error for single-qubit gates (e_1) and ISwap-like gates (e_2) has been reduced to 0.10% and 0.38%, respectively [as depicted in Figs. 2(a) and 2(b)], when all gates are applied simultaneously.

The performance of readout is another significant advancement in the Zuchongzhi 3.0. To achieve fast read-out with high fidelity, we increased the coupling strength between qubits and readout resonators to approximately 130 MHz and tuned the linewidths of the readout resonators to about 10 MHz. However, the increased coupling strength and linewidth result in a decrease in relaxation time. To address this, we optimized the design of the bandpass filter for dispersive qubit measurement, protecting the qubit from the Purcell effect. Furthermore, we employ a traveling-wave parametric amplifier to amplify the readout signal, thereby achieving superior readout performance.

Additionally, before each sampling task, we perform three rounds of measurement and apply the corresponding single-qubit gate to reset the qubit to the state $|0\rangle$. This method reduces the impact of thermal noise on state preparation and shortens the duration of each sampling. After these optimizations, the average readout error across 83 qubits has been suppressed to 0.87% [as depicted in Fig. 2(c)].

Large-scale random circuit sampling—After the initial calibration, we proceed with random quantum circuit sampling to evaluate the overall performance of the quantum processor. The random quantum circuit is designed in accordance with the method outlined in Ref. [27] to widen the performance gap between quantum computing and classical simulation. Notably, the two-qubit ISwap-like gates within each layer of two-qubit gates are
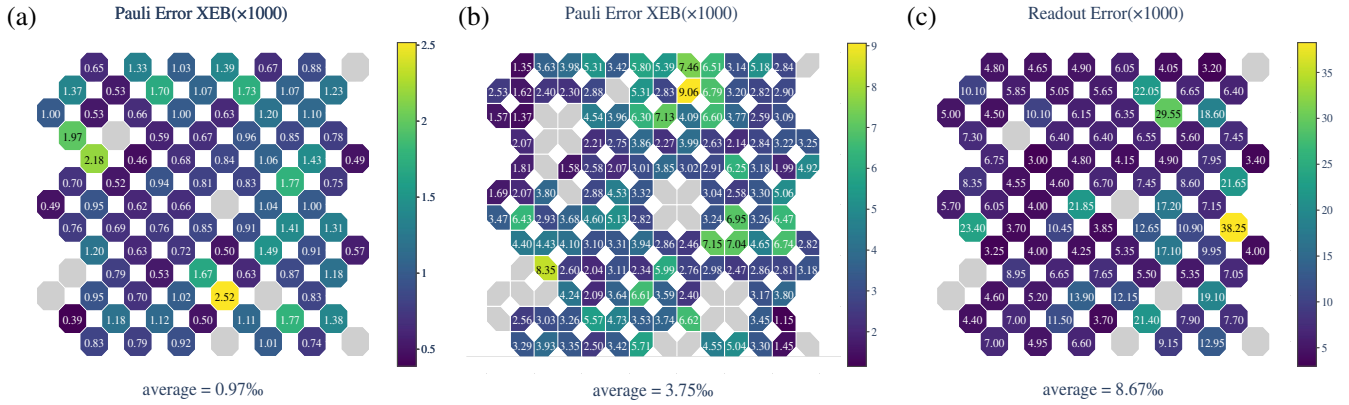
FIG. 2.   Gate and readout performance of the selected 83 qubits. (a) The single-qubit gate error, measured by the XEB experiment, has an average value of 0.97‰ and a duration of 28 ns. (b) The two-qubit gate error used in the experiment has an average value of 3.75‰ with a gate time of 45 ns. (c) The average readout error rate is 8.67‰, achieved through active reset and 0–2 state readout, which improves readout fidelity while reducing the sampling interval to 400 μs. The provided values correspond to the simultaneous operation of all selected qubits. For the detailed calibration data on the complete set of 105 qubits, refer to Supplemental Material [18].

applied following a specific pattern, denoted by A, B, C, and D, as illustrated in Fig. 3(a), and are executed in the sequence of $ABCD - CDAB$ in each cycle. The single-qubit gates in each cycle are selected at random from the set $\{\sqrt{X}, \sqrt{Y}, \sqrt{W}\}$.

Verifying the fidelity of the full random quantum circuit is challenging due to the inability to simulate its ideal output classically. To address this, patch circuits are utilized for the verification of large-scale random quantum circuits. These patch circuits are crafted by selectively removing a portion of the two-qubit gates between the patches. The entire circuit can be divided into two independent segments, termed as two patch, or into four segments, known as four patch. The

more divisions made, the more feasible the simulation becomes; however, the anticipated fidelity slightly increases due to the reduction in the number of two-qubit gates executed. We implement two-patch, four-patch, and the full version of the circuits, scaling from 12 to 32 cycles with 31 qubits each, and compute the linear XEB fidelities F_{XEB} for the respective output bit strings. The experimental results, as detailed in Fig. 3(b) (the results of the two patch are displayed in Fig. S7 in Supplemental Material [18]), reveal that the average fidelity ratios of the four-patch circuit to the full circuit fidelity is 1.05. This high degree of correspondence indicates the effectiveness of the verification circuits in ensuring the fidelity of quantum computations.
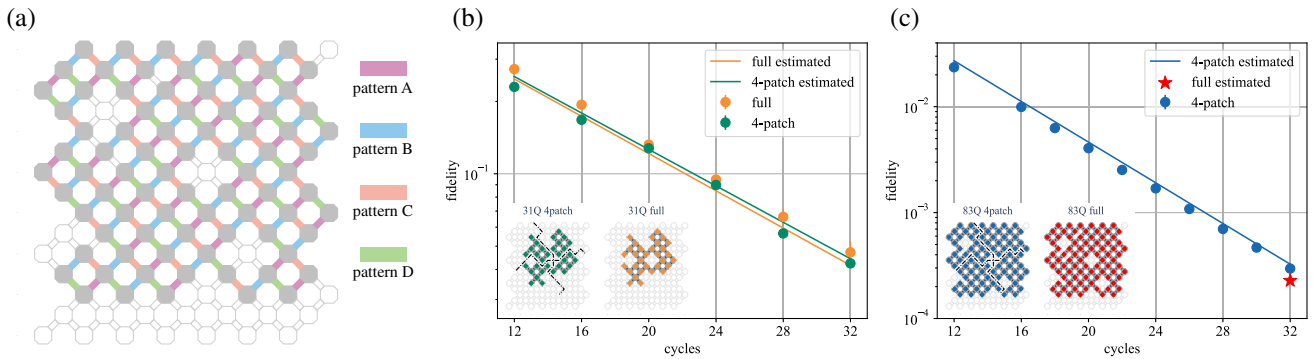

FIG. 3.   Experiment and estimate fidelity of random circuit sampling experiment for 31 qubits and 83 qubits. (a) The pattern diagram of the random circuit sampling experiment for 83 qubits. The ISwap-like gates are selected from the patterns labeled A, B, C, and D, arranged in the sequence $ABCDCDBA$. The gray octagons denote functional qubits, while purple, blue, orange, and green lines represent the ISwap-like gates associated with the four pattern A, B, C, D, respectively. Additionally, discarded qubits and couplers are indicated by empty octagons and lines. (b) The green and blue dots, respectively, represent the experimental values of the four-patch circuits and full circuits with 31 qubits over 12–32 cycles. The corresponding solid lines denote the estimated values for these circuits. The inserted topological diagram illustrates the specific configuration of 31 qubits. (c) The blue dots and line correspond to the experimental and estimated values, respectively, of the 83-qubit four-patch circuit. The red five-pointed star signifies the estimated value of the 83-qubit full circuit, where 410×10^6 bit strings are sampled. The inserted topological diagram depicts the specific configuration of 83 qubits. Error bars in (b) and (c) indicate the 5σ confidence intervals derived from statistical uncertainties.

Such an outstanding quantum processor allows us to run random circuit sampling on a larger scale than before. As shown in Fig. 3(c), we have achieved random circuit sampling of 83-qubit circuits with 12–32 cycles. For the largest full circuit featuring 83 qubits and 32 cycles, we have collected a total of approximately 4.1×10^8 bit strings. To assess its fidelity, we also gathered corresponding bit strings from four-patch circuits, which exhibit an experimental fidelity of 0.030%, while the estimated fidelity stands at 0.033%. This high degree of correspondence indicates that, even at a large scale of qubits and high circuit depth, employing the discrete error model to estimate fidelity remains highly reliable. Consequently, we can estimate the fidelity of the full circuit with 83 qubits and 32 cycles to be 0.023%.

Computational cost estimation—The current cutting-edge classical algorithm for simulating random quantum circuits is the tensor network algorithm [16,17,28–35]. We employ this method to evaluate the classical computational cost of our hardest circuit, featuring 83 qubits and 32 cycles. Considering memory constraints, we have examined the following two scenarios using a state-of-the-art method [16,17].

The first scenario involves capping the memory at 9.2 petabytes (PB), which is the memory size of the current most powerful supercomputer, Frontier. The estimated number of floating-point operations required to generate a million uncorrelated bit strings with a fidelity of 0.023% from an 83-qubit, 32-cycle random circuit using a classical computer is 7.7×10^{33}. In contrast, the latest quantum computational advantage experiment by Google [5], SYC-67, has an estimated classical simulation complexity of 4.7×10^{27} for replicating the same number of bit strings with fidelity that matches its experiment. Hence, the classical cost of simulating our most challenging random quantum circuit is 6 orders of magnitude higher than that of SYC-67. The progress on random circuit sampling is systematically summarized in Fig. 4. For our estimates, we utilize the specifications of the Frontier supercomputer, which boasts a theoretical peak performance of 1.685×10^{18} single-precision floating-point operations per second (FLOPS). We assume a 20% FLOP efficiency and take into account the low target fidelity of the simulation in the computational cost. Each single-precision complex FLOP necessitates eight machine FLOPs. Under these conditions, the projected time for classical simulation of our most challenging random quantum circuit is 5.9×10^9 yr using the current most powerful supercomputer, Frontier.

The complexity of tensor network algorithms is influenced by memory limitations, and we have further contemplated the scenario of virtually unlimited memory as an estimated lower bound for the sampling cost, although this situation is already unrealistic. By setting the memory limit to over 762.2 PB (considering both memory and total storage of Frontier as part of the memory), we estimate
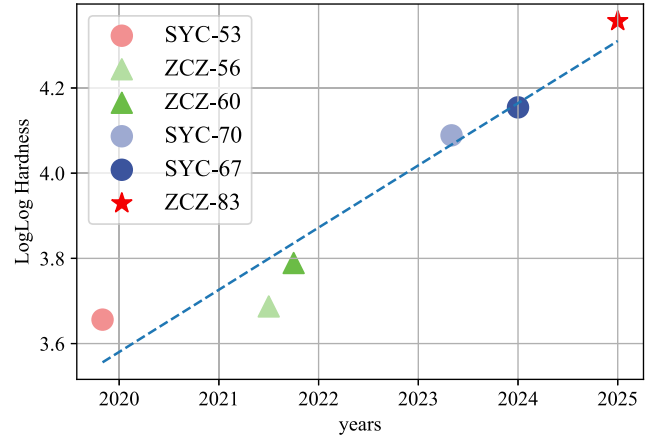

FIG. 4. Progress on random circuit sampling. The evolution of the time complexity in random circuit sampling experiments. The dotted line illustrates the pattern of doubly exponential growth. SYC and ZCZ, respectively, denote the Sycamore and Zuchongzhi processors.

the number of floating-point operations needed to generate a million uncorrelated bit strings of the same fidelity from our most challenging 83-qubit, 32-cycle random circuit remains high, at 6.9×10^{31}. Consequently, the estimated classical simulation time is an immense 5.2×10^7 yr, which underscores the robustness of our quantum advantage.

Conclusion—The Zuchongzhi 3.0, an advanced superconducting quantum computer prototype with its 105 qubits and exceptional operational fidelities, not only ups the ante in terms of the number of qubits but also enhances the precision of quantum manipulation. This dual advancement is key to expanding our quantum computing capabilities. Based on this robust platform, we have successfully executed a larger-scale random circuit sampling than previously achieved by Google [5], further widening the gap in computational capabilities between classical and quantum computing. Our work advances the discourse on quantum computing by providing empirical evidence of the technology's potential to revolutionize computational tasks. It serves as both a testament to the progress in quantum hardware and a foundation for practical applications. Scaling up in qubits and circuit complexity enhances our capacity to address sophisticated challenges in optimization [36,37], machine learning [38–43], and drug discovery [44–46].

Data availability—The data that support the findings of this article are openly available [47], embargo periods may apply.

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